REMARKS

This responds to the Office Action mailed on November 17, 2006. By this amendment, claim 10 is amended. No claims are canceled, or added. As a result, claims 1-15, 17-20, and 28-33 remain pending in this application.

§112 Rejection of the Claims

A. Rejection: Claims 10-15 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

B. Response: By this amendment, the recitation in claim 10, lines 20-21, to "...the circuit test apparatus under the control of the processor" has been eliminated to avoid confusion. As a result, claim 10 now overcomes the Examiner's rejection under 35 USC § 112, first paragraph. Claims 11-15, which depend from claim 10, now also overcome the Examiner's rejection under 35 USC § 112, first paragraph.

C. Rejection: Claims 10-15 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

D. Response: : By this amendment, the recitation in claim 10, lines 20-21, to "...the circuit test apparatus under the control of the processor" has been removed. Claim 10 now recites that the "...circuit test apparatus..." tests "...the spacing between the plane metallization layer and the pad associated with the signal carrying through hole..." As a result, claim 10 now overcomes the Examiner's rejection under 35 USC § 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The claim now more clearly indicates that the testing apparatus external to the device tests the device. As a result, claim 10 now overcomes the Examiner's

rejection under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention since the claim is now definite. Claims 11-15, which depend from claim 10, now also overcome the Examiner's rejection under 35 USC § 112, second paragraph.

§103 Rejection of the Claims

A. Rejection: Claims 1-9 and 28-33 were rejected under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505).

B. Response: In order for the Examiner to establish a prima facie case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference or references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. M.P.E.P. § 2142 (citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Claim 1 recites "...a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads...and a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer." As admitted by the Examiner, the Shiraki reference fails to teach a "test device having a probe tested on the PCB/device." (See page 6 of the Office Action dated November 17, 2006). The Examiner relies on the Ott et al. reference as showing the missing element. However, the Ott et al. reference fails to show such a tester. The tester of Ott et al. is always shown as testing conductive traces. The Ott et al. tester appears to teach a continuity tester. It appears that there is no teaching or suggestion of an arrangement which would test the spacing between the plane metallization layer from a signal carrying via through a

through hole that passes through the plane metallization layer, as recited and required by claim 1. Therefore, the combination falls short of the invention as claimed. In other words, the prior art references fail to teach or suggest all the claim limitations.

In addition, there does not appear to be any motivation for combining the references as suggested by the Examiner to yield applicant's invention. The Ott et al. reference tests for continuity of the electrical traces. There is no teaching of checking for spacing between a signal carrying line and a ground plane or plane metallization layer. The Examiner appears to be using the applicant's invention as a road map for combining references. Such Monday morning quarterbacking is improper application of 20/20 hindsight.

Even if one were to find proper motivation to combine the references, there would be no reasonable expectation of success, as required to make out a proper *prima facie* case of obviousness. The Shiraki reference teaches equally spaced through-holes 41 that attach to either a power plane metallization layer or to a ground plane metallization layer. The land 31 at the end of the through hole for the signal carrying line is not spaced on the same grid. Rather, the land 31 is spaced between four of the equally spaced through-holes. In other words, the land 31 is not on the grid of equally spaced through-holes. Ott et al. specifically teaches "...a uniform grid separation of the probes and two translator foils...". [See abstract of Ott et al. (U.S. 6,147,505)] Therefore, even if one was to combine the references as suggested by the Examiner, the equally spaced grid of Ott et al. would not electrically contact the land 31 of Shiraki (which is not positioned on a grid). Therefore, the combination would not work since the grid of Ott et al. would not contact the land 31.

For all of the above-stated reasons, claim 1 overcomes the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505). Claims 2-9 depend from claim 1 and include the limitations of claim 1 by their dependency. As a result, claims 2-9 now also overcome the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505) for the same reasons as set forth above with respect to claim 1.

Claim 28 recites "...a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer." Claim 28 overcomes the rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S.

6,147,505) for the same reasons as set forth above with respect to claim 1. Claims 29-33 depend from claim 28 and include the limitations of claim 28 by their dependency. As a result, claims 29-33 now also overcome the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505).

C. Rejection: Claims 10-15 were rejected under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690), and further in view of Ott et al. (U.S. 6,147,505).

D. Response: In order for the Examiner to establish a prima facie case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference or references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. M.P.E.P. § 2142 (citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Claim 10 recites "...a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads; and a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole." The Examiner admits that neither the Shiraki or Conn et al. "...disclose the signal through hole (21) connected to a test apparatus." (see page 8 of the Office Action dated November 17, 2006). Applicant notes that the Examiner admitted that Shiraki does not teach a tester (see page 5 of the Office Action dated November 17, 2006). Conn et. al. also fails to set forth or teach a tester. A word search conducted on Conn et al. (US Patent No. 5, 418,690) on the USPTO website that failed to yield any hits for the word "test" or "tester" supports the fact that Conn et al. also fails to teach a tester of any sort.

Therefore, Conn et al. shows a circuit board 10 that includes memory 12, 13 and a processor 11. However, the resulting device from combining Shiraki and Conn et al. fails to teach a tester. The structure associated with the through-holes in the device is shown in Shiraki. Conn et al. fails to teach any other type of structure.

Adding Ott et al. does not make claim 10 obvious. The Ott et al. reference fails to show a tester of the type recited in claim 10. The tester of Ott et al. is always shown as testing conductive traces. The Ott et al. tester appears to teach a continuity tester. It appears that there is no teaching or suggestion of an arrangement which would test the spacing between the plane metallization layer and the pad associated with the signal carrying through hole, as recited and required by claim 10. Therefore, the combination falls short of the invention as claimed. In other words, the prior art references fail to teach or suggest all the claim limitations.

In addition, there does not appear to be any motivation for combining the references as suggested by the Examiner to yield applicant's invention. The Ott et al. reference tests for continuity of the electrical traces. There is no teaching of checking for spacing between a signal carrying line and a ground plane or plane metallization layer. The Examiner appears to be using the applicant's invention as a road map for combining references. Application of 20/20 hindsight is improper.

Even if one were to find proper motivation to combine the references, there would be no reasonable expectation of success, as required to make out a proper *prima facie* case of obviousness. The Shiraki reference teaches equally spaced through-holes 41 that attach to either a power plane metallization layer or to a ground plane metallization layer. The land 31 at the end of the through hole for the signal carrying line is not spaced on the same grid. Rather, the land 31 is spaced between four of the equally spaced through-holes. In other words, the land 31 is not on the grid of equally spaced through-holes. Ott et al. specifically teaches "...a uniform grid separation of the probes and two translator foils...". [See abstract of Ott et al. (U.S. 6,147,505)] Therefore, even if one was to combine the references as suggested by the Examiner, the equally spaced grid of Ott et al. would not electrically contact the land 31 of Shiraki (which is not positioned on a grid). Therefore, the combination would not work since the grid of Ott et al. would not contact the land 31.

For all of the above-stated reasons, claim 10 overcomes the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690), and further in view of Ott et al. (U.S. 6,147,505). Claims 11-15 depend from claim 10 and include the limitations of claim 10 by their dependency. As a result, claims 11-15 now also overcome the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690), and further in view of Ott et al. (U.S. 6,147,505) for the same reasons as set forth above with respect to claim 10.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6977) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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